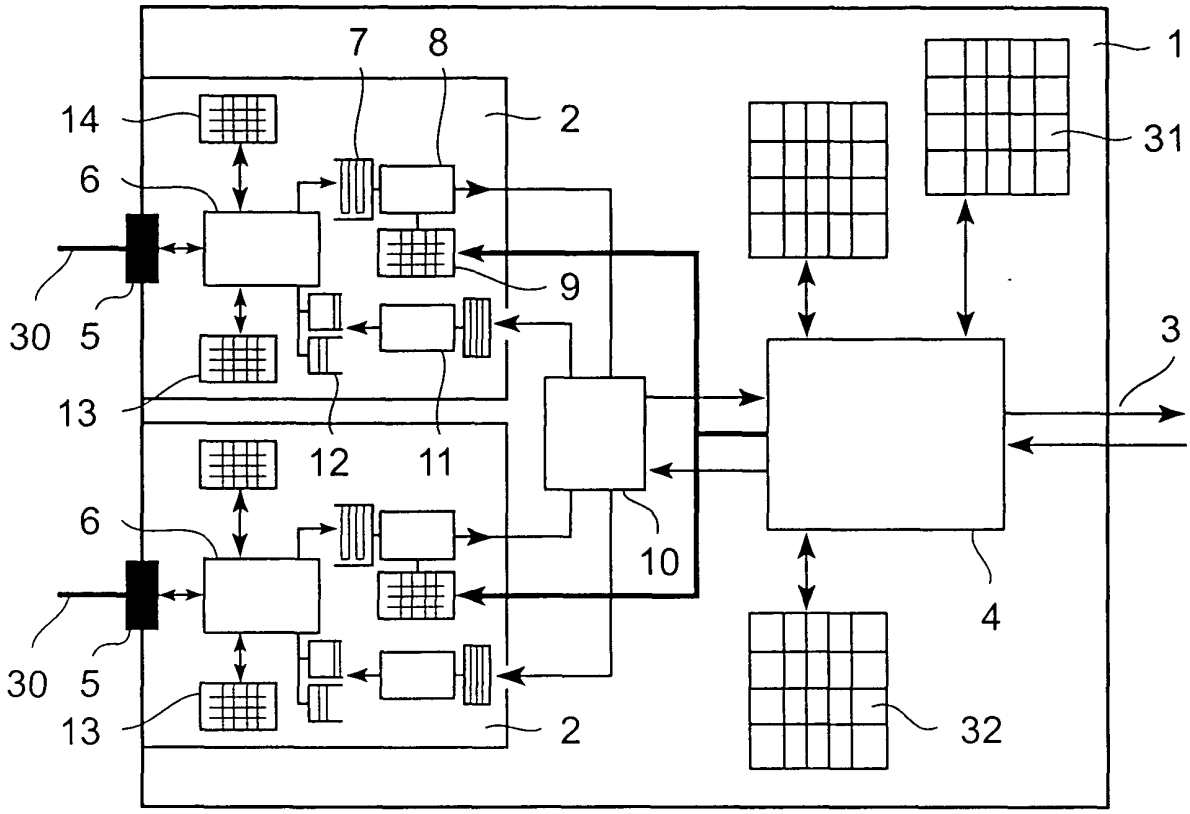


Fig. 1

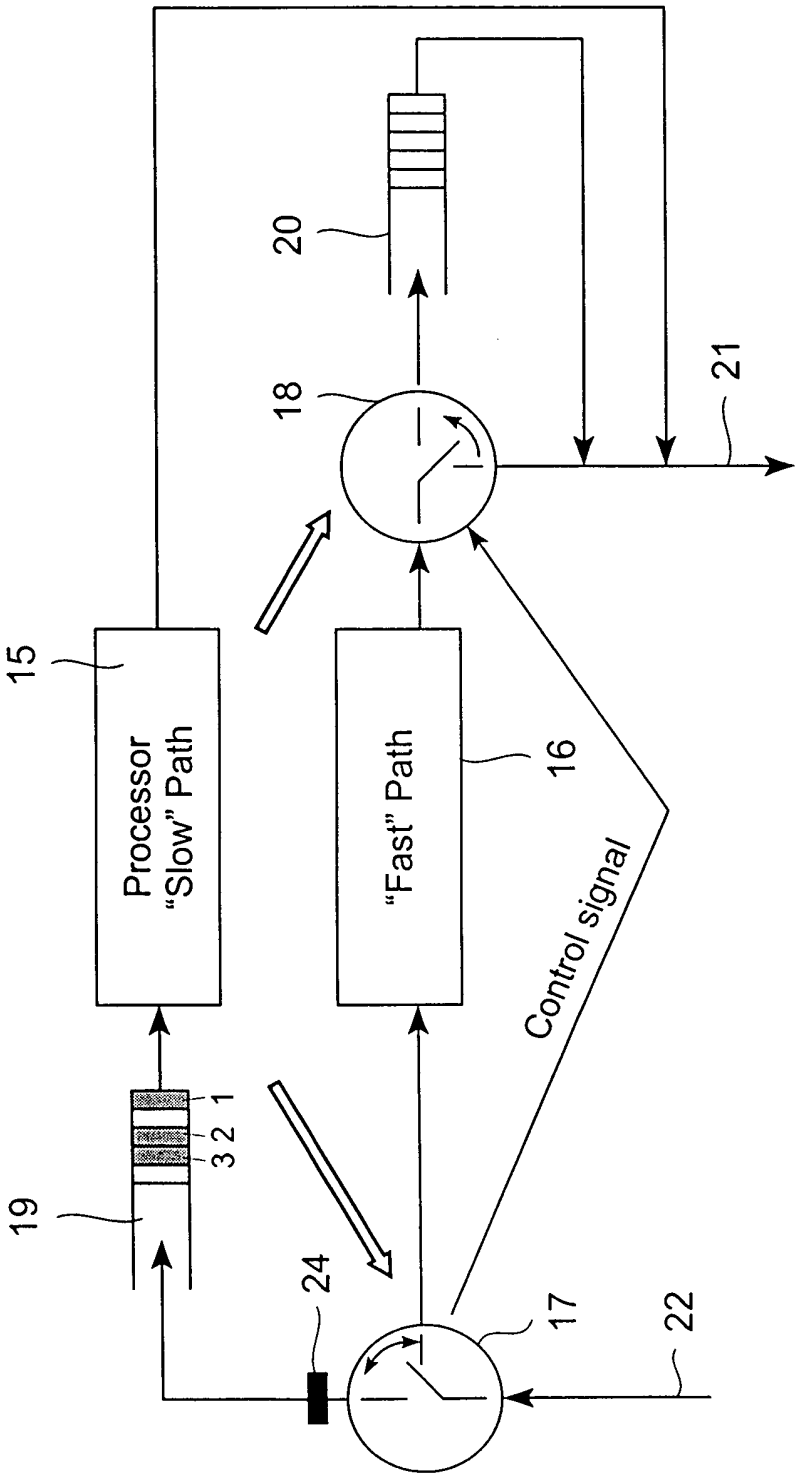

20
18
21
15
Processor
"Slow" Path
"Fast" Path
16
Control signal
3 2 1
19
24
17
22

Fig. 2

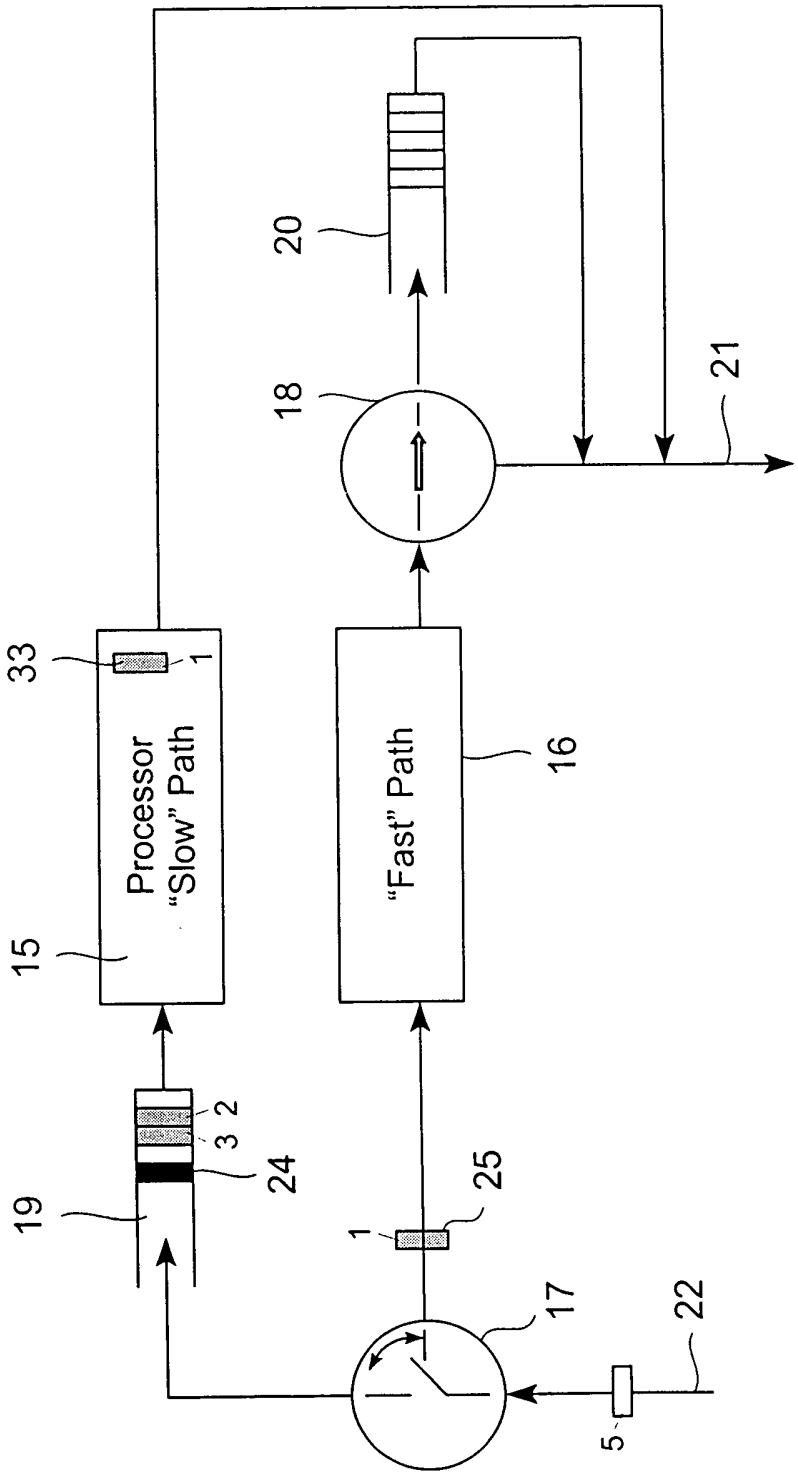

20
18
21
33
1
Processor
"Slow" Path
15
"Fast" Path
16
3 2
24
19
25
1
17
22
5

Fig. 3

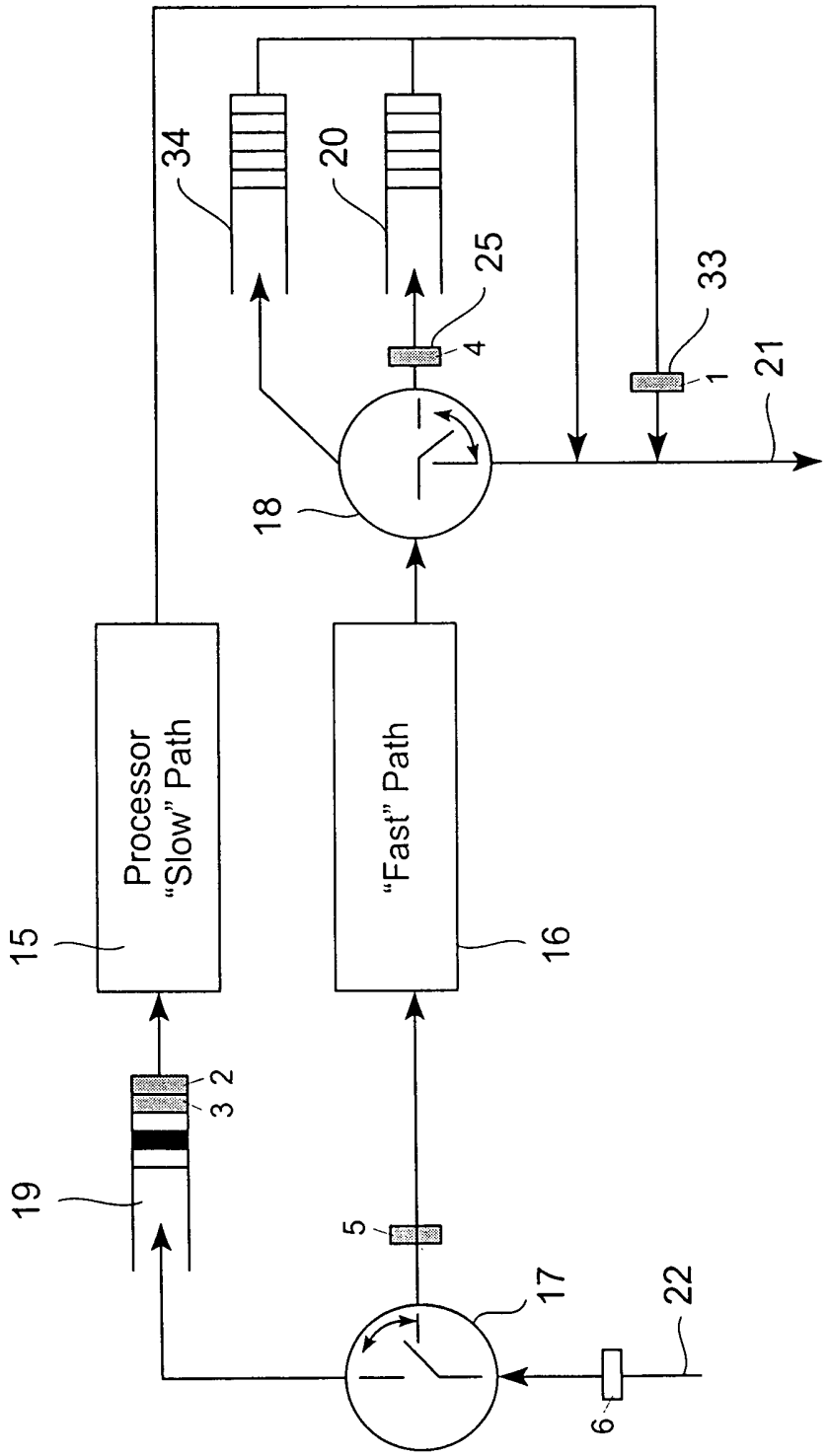

34
20
25
33
4
1
21
18
Processor "Slow" Path
"Fast" Path
15
16
3 2
19
5
17
22
6

Fig. 4

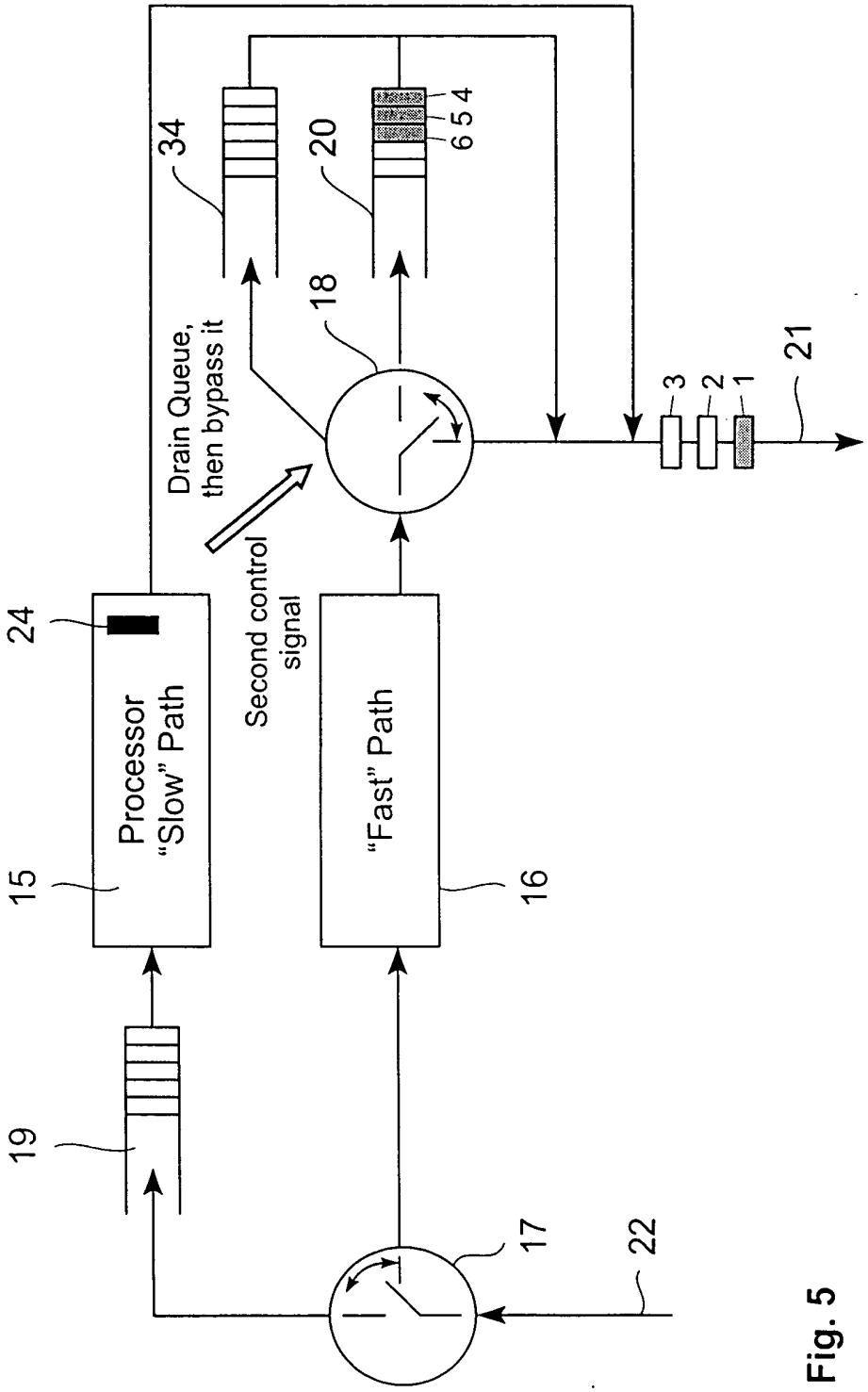

34
20
6 5 4
18
Drain Queue, then bypass it
Second control signal
3
2
1
21
24
Processor "Slow" Path
15
"Fast" Path
16
19
17
22

Fig. 5

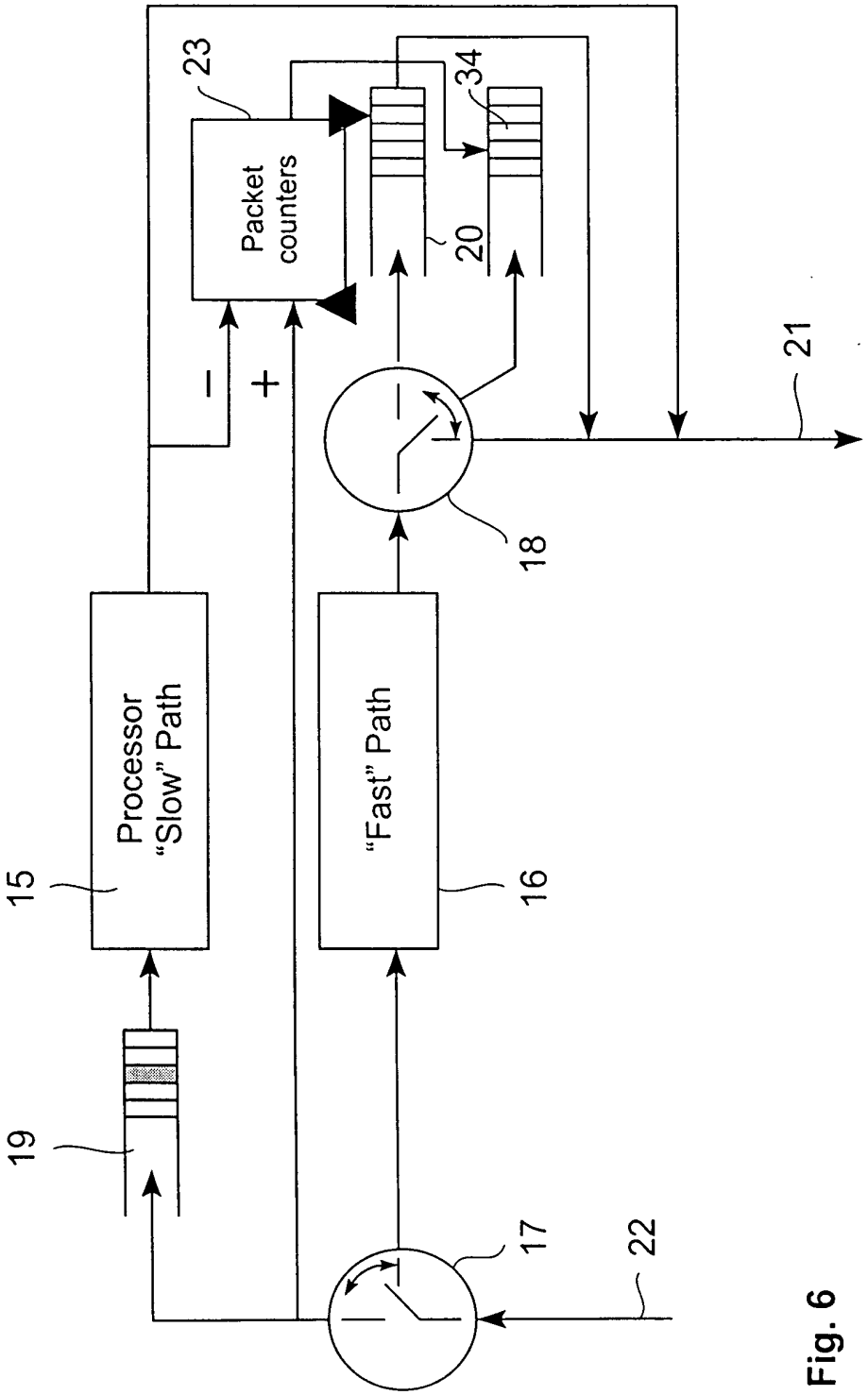

23
Packet counters
34
20
21
18
Processor "Slow" Path
"Fast" Path
15
16
19
17
22

Fig. 6

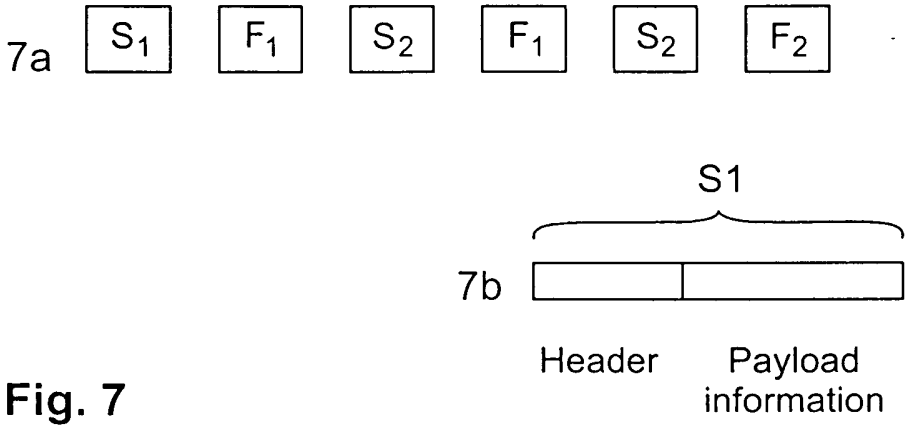
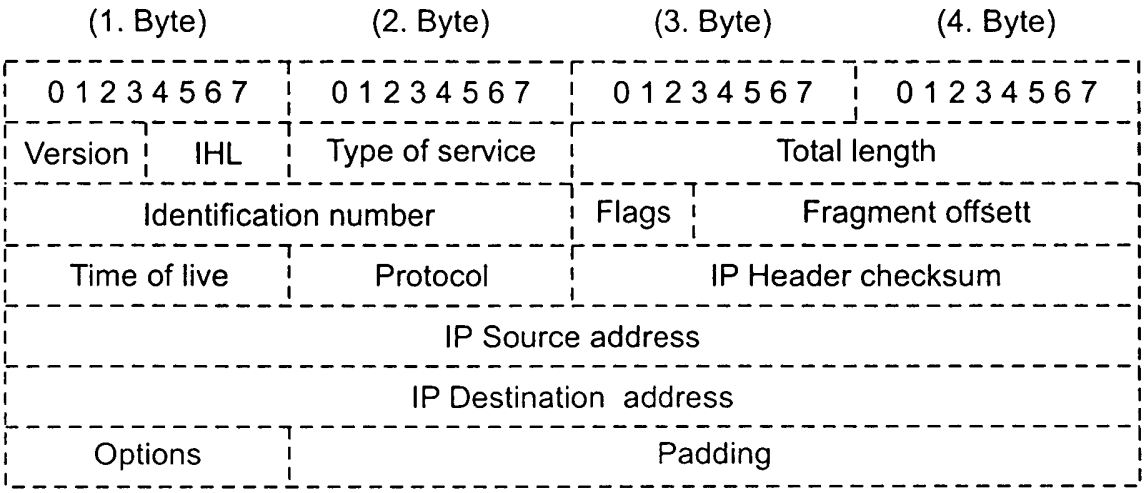


Fig. 7



Total length

Fig. 8